IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)
	)
KUROKAWA et al.	)
	) Art Unit 2186
Application Number: 10/765,098	)
	)
Filed: January 28, 2004	)
	)
For: STORAGE SYSTEM WITH	)
A DATA SORT FUNCTION	)
	)
Attorney Docket No. WILL.0003	)

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

COVER LETTER

Sir:

[x]   The fee for submission of claims is calculated as shown below:

FOR	TOTAL WITH NEW CLAIMS ADDED	TOTAL CURRENTLY ON FILE	CLAIMS PAID	RATE	CALCULATION
Total Claims	10	10	(Over 20)	x $50	0
Independent Claims	2	2	(Over 3)	x $200	0
MULTIPLE DEPENDENT CLAIM(S)				+ $360	0
REDUCTION FOR FILING BY SMALL ENTITY (note 37 C.F.R. §§ 1.9, 1.27, 1.28). IF APPLICABLE, VERIFIED STATEMENT MUST BE ATTACHED				x ½	
				TOTAL	0.00

In addition, the below-identified communications are submitted in the above-captioned application or proceeding:

[ ] Preliminary Amendment
     (with Claim Amendments)
[ ] Substitute Specification
[ ] Assignment
[x] Statements & Pre-exam search report with
     References

[ ] Terminal Disclaimer
[ ] Letter to Draftsperson
[x] Information Disclosure Statement
[x] Petition to Make Special under 37 CFR
     §1.102(d) for Accelerated Examination

[ ]   Please charge my **Deposit Account Number** _____ in the amount of _____ to cover the
       fees for _____. A duplicate copy of this paper is enclosed.

[x] A check in the amount of **$130.00** to cover the petition fee is enclosed.

[x] The Commissioner is hereby authorized to charge any additional fees associated with this
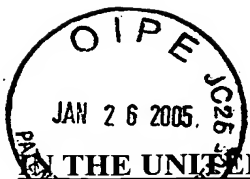   communication, or credit any overpayment to **Deposit Account Number 08-1480**.

                                    Respectfully submitted,

                          _____
                          Stanley P. Fisher
                          Registration Number 24,344

                          Juan Carlos A. Marquez
                          Registration No. 34,072

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January 26, 2005

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PETITION TO MAKE SPECIAL UNDER 37 C.F.R. § 1.102(d)

FOR ACCELERATED EXAMINATION

Sir:

Pursuant to 37 C.F.R. § 1.102(d), Applicant respectively requests the application to be examined on the merits in conjunction with the pre-examination search results, the detailed discussion of the relevance of the results and amendments as filed concurrently.

Substantive consideration of the claims is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

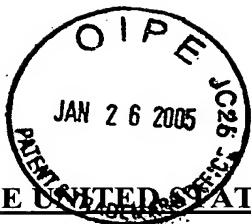Stanley P. Fisher
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January 25, 2005
SPF/JCM/JT

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STATEMENTS & PRE-EXAMINATION SEARCH REPORT
SUPPLEMENTAL TO
THE PETITION TO MAKE SPECIAL

Sir:

Pursuant to 37 C.F.R. §§ 1.102 and MPEP 708.02 VIII, Applicant hereby submits that (1) all claims of record are directed to a single invention, or if the Office determines that all the claims presented are not obviously directed to a single invention, will make an election without traverse as a prerequisite to the grant of special status; (2) a pre-examination search has been conducted according to the following field of search; (3) copies of each reference deemed most closely related to the subject matter encompassed by the claims are enclosed; and (4) a detailed discussion of the references pointing out how the claimed subject matter is patentable over the references is also enclosed herewith.

FIELD OF THE SEARCH

The field of search covered Class 711, subclasses 100 (U.S. & Foreign) and 112 (U.S. & Foreign). Additionally, a computer database search was conducted on the USPTO systems EAST and WEST for U.S. and foreign patents; a keyword search was conducted in Class 707, subclasses 1, 3, 7 and 100; Class 710, subclasses 5, 6 and 39; and Class 711, subclasses 111, 113, 114, 158 and 170; and a literature search was also conducted on the internet and

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commercial databases for relevant non-patent documents. Examiner Reginald Bragdon in Class 711 (Art Unit 2188) was consulted in confirming the field of search.

The search was directed towards data processing (e.g., transfer/copying) system having a plurality of storage systems. In particular, the search was directed to a storage system with a data sort function. In particular, the search was directed towards claims 1-10 of U.S. Application Number 10/765098. The claims describe a storage system, connectable via a communication channel to one or more host devices, comprising an external storage device having one or more physical devices to store data for input from and output to the host device and a storage control device which controls transfer of the data between the host device and the external storage device, wherein, the storage control device has cache memory which temporarily holds one or more blocks of the data, control information memory which stores control information, and a control portion which is connected to the host devices, the external storage device, the cache memory, and the control information memory, defines each of one or more sets of blocks of the data stored in the external storage device; the control portion has one or more processors which receive sort processing execution instructions from the host device and perform sort processing; the one or more processors are notified, by means of the sort processing execution instruction, of sort-in information, key information, sort-work information , and sort-out information; and the one or more processors, when executing the sort processing, write a specified sort-in block group in the external storage device to the cache memory, and sort the sort-in block group written to the cache memory based on the specified sort key value, store the sorted sort-in block group, and notify the host device of the completion of the sort processing. The storage system comprises the storage control device having shared memory, which can be used for different prescribed purposes and a control portion, which is connected to the host device, and as further claimed in the disclosure.

The search revealed the following U.S. patents, which are listed for convenience:

U.S. Patent Number	Inventor(s)
5,343,427	Teruyama
5,652,857	Shimoi et al.
5,860,083	Sukegawa
6,230,220	Cohen et al.
6,424,970	Arakawa et al.
6,571,244	Larson

Published Patent Application	Inventor(s)
2002/0065793	Arakawa et al.
2003/0061407	Kurokawa et al.
2003/0163457	Yano et al.
2004/0039869	Kurokawa et al.
2004/0098538	Horn et al.
2004/0098543	Araki et al.
2004/0205303	Naveh et al.

Foreign Patent Number	Inventor(s)
JP 10-078967	Ishiai

Discussion of References:

U.S. Patent Application Number 2004/0039869 of **Kurokawa** et al. is assigned to Hitachi Ltd. and entitled "Information Processing System." **Kurokawa's** information processing system (Fig. 1) includes a host processing device 10, an external storage device 13 that uses one or more physical devices 131 to store data that are subjects of input/output requests from the host processing device 10, and a control device 12 intervening between the host processing device 10 and the external storage device 13 and that controls data receiving and sending. However, **Kurokawa** is silent about any sorting operation such that **Kurokawa's** control device 12 does not have "one or more processors which receive sort

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processing execution instructions from said host devices and perform sort processing" as now recited in claim 1. As such, **Kurokawa's** control device 12 does not have "one or more processors are notified, by means of said sort processing execution instructions, of sort-in information specifying an arbitrary block group within an arbitrary logical device as a sort-in block group, key information specifying data at an arbitrary position in said blocks as a sort key, sort-work information specifying an arbitrary block group in an arbitrary logical device as a sort-work block group, and sort-out information specifying an arbitrary block group in an arbitrary logical device as a sort-out block group," or any processors "write said specified sort-in block group in said external storage device to said cache memory, and while using said specified sort-work block group as a work area, sort said sort-in block group written to said cache memory based on said specified sort key value, store said sorted sort-in block group to said specified sort-out block group, and notify said host devices of the completion of said sort processing" as now recited in claim 1. U.S. Patent Application Numbers 2003/0061407 of Kurokawa et al. shares the same deficiencies.

U.S. Patent Application Number 2003/0163457 of **Yano** et al. is assigned to Hitachi Ltd. and entitled "Storage System." **Yano's** storage system includes a plurality of storage physical devices 102-106, means for controlling access to the plurality of storage physical devices 102-106, an interface respectively provided between a host device 114 or 115 and the storage physical devices 102-106, and setting means for selecting a specific storage physical device from the plurality of storage physical devices, based on predetermined conditions and placing data blocks therein. The cache memory 111 temporarily stores therein data written from each host device 114 or 115 to carry out an access process from the host device 114 or 115 at high speed, or stores therein data read immediately before. However, **Yano** is silent about any sorting operation such that **Yano's** disk controller 109 does not have "one or more processors which receive sort processing execution instructions from said host devices and perform sort processing" as now recited in claim 1. As such, **Yano's** processor 110 is not "notified, by means of said sort processing execution instructions, of sort-in information specifying an arbitrary block group within an arbitrary logical device as a sort-in block group, key information specifying data at an arbitrary position in said blocks as a sort key, sort-work information specifying an arbitrary block group in an arbitrary logical device as a sort-work block group, and sort-out information specifying an arbitrary block group in an arbitrary logical device as a sort-out block group," or does not "write said specified sort-in block group

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in said external storage device to said cache memory, and while using said specified sort-work block group as a work area, sort said sort-in block group written to said cache memory based on said specified sort key value, store said sorted sort-in block group to said specified sort-out block group, and notify said host devices of the completion of said sort processing" as now recited in claim 1.

U.S. Patent Application Number 2002/0065793 of **Arakawa** et al. is assigned to Hitachi Ltd. and entitled "Sorting System And Method Executed By Plural Computers For Sorting And Distributing Data To Selected Output Nodes." **Arakawa's** sorting system (Fig. 1) includes a plurality of input nodes/computers 100 (Abstract); one output node 300; and a shared external storage 500 unit connected between each of the input units 100 and the output unit 300, wherein, each of the input units 100 for sorting a input local disk 200 therein comprises a first buffer 110; means for storing sorting target data in the first buffer 100; means for internally sorting data in the first buffer 100 in accordance with a predetermined sorting rule; and means for storing as a sorted string an internally sorted result in the shared external storage unit 500. In short, **Arakawa** has a two-level sorting scheme: In level I, each of the input units 100 sorts data in its input local disk 200 thereby processing in parallel all input data in a plurality of computers (nodes) to shorten processing time (Abstract). In level II, the output node 300 reads the sorted string from the shared disk 500 and merges it and outputs a whole sorted result of all input data to an output local disk 400. Each of **Arakawa's** input units 100 sorts independently. **Arakawa** has shared disk 500 and shared output note/computer 300, but not a shared storage control device 12 connecting between host devices 1 and an external storage device 11 for coordinating its plurality of processors with a shared cached memory 123 thereby performing an one-level sorting scheme. **Arakawa** simply does not provide such a "storage control device 12 having cache memory which temporarily holds one or more blocks of said data, control information memory which stores control information, and a control portion which is connected to said host devices, said external storage device, said cache memory, and said control information memory, defines each of one or more sets of blocks of said data stored in said external storage device as one or more logical devices, and controls the input and output of said blocks to and from said external storage device, said cache memory, and said host devices" as now recited in claim 1. In addition, **Arakawa's** input note CPUs 101 are not "notified, by means of said sort processing execution instructions, of sort-in information specifying an arbitrary block group

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within an arbitrary logical device as a sort-in block group, key information specifying data at an arbitrary position in said blocks as a sort key, sort-work information specifying an arbitrary block group in an arbitrary logical device as a sort-work block group, and sort-out information specifying an arbitrary block group in an arbitrary logical device as a sort-out block group", and they do not "write said specified sort-in block group in said external storage device to said cache memory, and while using said specified sort-work block group as a work area, sort said sort-in block group written to said cache memory based on said specified sort key value, store said sorted sort-in block group to said specified sort-out block group, and notify said host devices of the completion of said sort processing" as now recited in claim 1. US Pat. No. 6,424,970 to Arakawa et al. shares the same deficiencies.

U.S. Patent Application Number 2004/0098543 of **Araki** et al. is assigned to Hitachi Ltd. and entitled "Storage System." **Araki** (Fig. 1) shows storage system coupled to a plurality of host processors 10 and service equipment 13. The storage system includes an external storage device 14 and a control unit 12 for controlling transfer of information between the host processors 10 and the external storage device 14. The system includes host adaptors 122, which write the received data in the cache memory 121 and send a write command end message indicating completion of the write request to the host processor 10. The disk adaptors 123 transfer the data stored temporarily in the cache memory 121 to the logical device 143 to be written at a location indicated by the write request. However, **Araki** is silent about any sorting operation such that **Araki's** control unit 12 does not have "one or more processors which receive sort processing execution instructions from said host devices and perform sort processing" as now recited in claim 1. As such, **Araki's** control unit 12 does not have "one or more processors are notified, by means of said sort processing execution instructions, of sort-in information specifying an arbitrary block group within an arbitrary logical device as a sort-in block group, key information specifying data at an arbitrary position in said blocks as a sort key, sort-work information specifying an arbitrary block group in an arbitrary logical device as a sort-work block group, and sort-out information specifying an arbitrary block group in an arbitrary logical device as a sort-out block group," or any processors "write said specified sort-in block group in said external storage device to said cache memory, and while using said specified sort-work block group as a work area, sort said sort-in block group written to said cache memory based on said specified sort key value,

store said sorted sort-in block group to said specified sort-out block group, and notify said host devices of the completion of said sort processing" as now recited in claim 1.

U.S. Patent Numbers 5,343,427 (Teruyama), 5,652,857 (Shimoi et al.), 5,860,083 (Sukegawa), 6,230,220 (Cohen et al.), 6,571,244 (Larson), U.S. Patent Application Numbers 2004/0098538 (Horn et al.), 2004/0205303 (Naveh et al.) and Japanese Patent Number 10078967 (Ishiai) each merely show a general storage system having external storage devices, physical devices storing data, and sorting processes. However, they all fail to provide "a control device 12 connecting between host devices 1 and an external storage device 11 for coordinating its plurality of processors with a shared cached memory 123 thereby executing sort processing execution instructions received from said host devices and perform sort processing" as recited in claim 1. In addition, they all fail to provide any processors in the control device 12 which are "notified, by means of said sort processing execution instructions, of sort-in information specifying an arbitrary block group within an arbitrary logical device as a sort-in block group, key information specifying data at an arbitrary position in said blocks as a sort key, sort-work information specifying an arbitrary block group in an arbitrary logical device as a sort-work block group, and sort-out information specifying an arbitrary block group in an arbitrary logical device as a sort-out block group", and which "write said specified sort-in block group in said external storage device to said cache memory, and while using said specified sort-work block group as a work area, sort said sort-in block group written to said cache memory based on said specified sort key value, store said sorted sort-in block group to said specified sort-out block group, and notify said host devices of the completion of said sort processing" as now recited in claim 1.

CONCLUSION

Based on the results of the comprehensive prior art search as discussed above, Applicants contend that the position calculation method as now recited in independent claim 1, especially the features of "a control device 12 connecting between host devices 1 and an external storage device 11 for coordinating its plurality of processors with a shared cached memory 123 thereby executing sort processing execution instructions received from said host devices and perform sort processing," "the control device 12 having one or more processors which are notified, by means of said sort processing execution instructions, of sort-in information specifying an arbitrary block group within an arbitrary logical device as a sort-in

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block group, key information specifying data at an arbitrary position in said blocks as a sort key, sort-work information specifying an arbitrary block group in an arbitrary logical device as a sort-work block group, and sort-out information specifying an arbitrary block group in an arbitrary logical device as a sort-out block group," and "the processors write said specified sort-in block group in said external storage device to said cache memory, and while using said specified sort-work block group as a work area, sort said sort-in block group written to said cache memory based on said specified sort key value, store said sorted sort-in block group to said specified sort-out block group, and notify said host devices of the completion of said sort processing" are patentably distinct from the cited prior art references.

In particular, as now recited in the claim 1 (e.g., Fig. 1), the storage system, connectable via a communication channel 3 to one or more host devices 1, comprising an external storage device 11 having one or more physical devices to store data for input from and output to said host devices 1 and a storage control device 12 which controls transfer of said data between said host devices 1 and said external storage device 11. The storage control device 12 has cache memory 123 which temporarily holds one or more blocks of said data, control information memory 122 which stores control information, and a control portion 121 which is connected to said host devices 1, said external storage device 11, said cache memory 123, and said control information memory 122, defines each of one or more sets of blocks of said data stored in said external storage device 11 as one or more logical devices 112, and controls the input and output of said blocks to and from said external storage device 11, said cache memory 123, and said host devices 1. The control portion 121 has one or more processors which receive sort processing execution instructions 30 from said host devices 1 and perform sort processing. The one or more processors are notified, by means of said sort processing execution instructions 30 (Fig. 3), of sort-in information specifying an arbitrary block group within (a sort range 302 of) an arbitrary logical device (at a sort-in address 301) as a sort-in block group, key information specifying data at an arbitrary position (at a key position 304) in said blocks as a sort key 303, sort-work information specifying an arbitrary block group in (a sort-out range 306 of) an arbitrary logical device (at a sort-out address 305) as a sort-work block group, and sort-out information specifying an arbitrary block group in (a sort-work range 308 of) an arbitrary logical device (at a sort-work address 307) as a sort-out block group. The one or more processors, when executing said sort processing in response to said sort processing execution instructions 30, write said specified sort-in block group in said

external storage device 11 to said cache memory 123, and while using said specified sort-work block group as a work area, sort said sort-in block group written to said cache memory 123 based on said specified sort key value 303, store said sorted sort-in block group to said specified sort-out block group, and notify said host devices 1 of the completion of said sort processing.
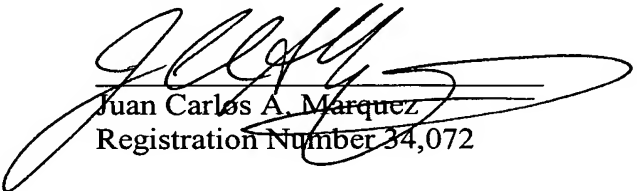
The invention is also directed to a storage system, as now recited in claim 10 (reciting all essential elements of claim 1), connectable via a communication channel 3 to one or more host devices 1, comprising an external storage device 11 which stores data for input from and output to said host devices, and a storage control device 12 which controls transfer of said data between said host devices 1 and said external storage device 11. The storage control device 12 has shared memory 122, 123 which can be used for different prescribed purposes and a control portion 121 which is connected to said host devices 1, said external storage device 11, and said shared memory 122, 123, and controls data input to and output from said external storage device 11, said host devices 1, and said shared memory 122, 123. The control portion 121 has one or more processors which receive sort processing execution instructions 30 from said host devices 11 and perform sort processing. The one or more processors perform sort processing in which a first storage area in said external storage device 11 is selected as a sort-in area, a second storage area in said external storage device 11 or said shared memory 122, 123 is selected as a sort-work area, a third storage area in said external storage device 11 is selected as a sort-out area, the data of said sort-in area is sorted using said sort-work area, and the sorted data is stored in said sort-out area.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references, Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable consideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,

_____
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